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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Andrew Harvery Barr et al.	Examiner:	Jeremy C. Norris
Serial No.:	10/621,925	Group Art Unit:	2841
Filed:	July 17, 2003	Docket No.:	200308576-1
Title:	ALTERNATING VOIDED AREAS OF ANTI-PADS		

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HEWLETT-PACKARD COMPANY
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PATENT APPLICATION

ATTORNEY DOCKET NO. 200308576-1IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Harvey Barr et al.

Confirmation No.: 2574

Application No.: 10/621,925

Examiner: Jeremy C. Norris

Filing Date: July 17, 2003

Group Art Unit: 2841

Title: ALTERNATING VOIDED AREAS OF ANTI-PADS

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TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on April 7, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) \$500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:☐ 1st Month
\$120☐ 2nd Month
\$450☐ 3rd Month
\$1020☐ 4th Month
\$1590☐ The extension fee has already been filed in this application.☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.Please charge to Deposit Account 08-2025 the sum of \$ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
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Respectfully submitted,

Andrew Harvey Barr et al.

By: 

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Rev 10/05 (ApI Brief)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Andrew Harvey Barr	Examiner:	Jeremy C. Norris
Serial No.:	10/621,925	Group Art Unit:	2841
Filed:	July 17, 2003	Docket No.:	200308576-1
Title:	ALTERNATING VOIDED AREAS OF ANTI-PADS		

APPEAL BRIEF UNDER 37 C.F.R. §41.37

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Commissioner for Patents
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Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on April 7, 2006, appealing the final rejection of claims 1-31 of the above-identified application as set forth in the Final Office Action mailed December 12, 2005.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of \$500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. §41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-31.

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Appeal Brief to the Board of Patent Appeals and Interferences

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Serial No.: 10/621,925

Filed: July 17, 2003

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REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed December 12, 2005, claims 1-31 were finally rejected. Claims 1-31 are pending in the application, and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed December 12, 2005. A Response After Final was filed on February 13, 2006, but no amendments to the claims were proposed by Appellant or entered by the Examiner.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The subject matter of the independent claims involved in the Appeal is related to circuit boards having anti-pads around via signal barrels where the anti-pads include alternating voided areas.

One aspect of the present invention, as claimed in independent claim 1, provides a printed circuit board (110). The printed circuit board (110) includes a first conductive plane (20) and a second conductive plane (20') substantially parallel to the first conductive plane (20). A via signal barrel (10) transects the first (20) and second (20') conductive planes. A first anti-pad (400, 500) is positioned between the first conductive plane (20) and the via signal barrel (10). The first anti-pad (400, 500) has a first voided area (210) and a first non-

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voided area (200). A second anti-pad (400', 500') is positioned between the second conductive plane (20') and the via signal barrel (10). The second anti-pad (400', 500') has a second voided area (210') and a second non-voided area (200'). The first voided area (210) does not completely overlap the second voided area (210'). *See Specification*, at page 8, line 5 through page 9, line 20; and Figures 6 and 7.

Another aspect of the present invention, as claimed in independent claim 8, provides a printed circuit board (110). The printed circuit board (110) includes a first conductive plane (20) and a second conductive plane (20') substantially parallel to the first conductive plane (20). A via signal barrel (10) transects the first (20) and second (20') conductive planes. A first partially voided anti-pad (400, 500) is positioned between the first conductive plane (20) and the via signal barrel (10). The first partially voided anti-pad (400, 500) has a first pattern and a first orientation. A second partially voided anti-pad (400', 500') is positioned between the second conductive plane (20') and the via signal barrel (10). The second partially voided anti-pad (400', 500') has a second pattern and a second orientation. The first orientation is offset from the second orientation. *See specification*, at page 8, line 5 through page 9, line 20; and Figures 6 and 7.

Yet another aspect of the present invention, as claimed in independent claim 15, provides a printed circuit board (110). The printed circuit board (110) includes a first conductive plane (20) and a second conductive plane (20') substantially parallel to the first conductive plane (20). A first via signal barrel (10) transects the first (20) and second (20') conductive planes. A first anti-pad (600) is positioned between the first conductive plane (20) and the first via signal barrel (10). The first anti-pad (600) has a first length and a first width and a first orientation. A second anti-pad (600') is positioned between the second conductive plane (20') and the first via signal barrel (10). The second anti-pad (600') has a second length and a second width and a second orientation. The first orientation is offset from the second orientation. *See specification*, at page 9, line 21 through page 11, line 2; and Figures 8-10.

Yet another aspect of the present invention, as claimed in independent claim 24, provides a method for forming a printed circuit board (110). The method includes providing a first conductive plane (20) and providing a second conductive plane (20') substantially parallel to the first conductive plane (20). The method further includes forming a via signal

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barrel (10) transecting the first (20) and second (20') conductive planes. The method further includes forming a first anti-pad (400, 500, 600) positioned between the first conductive plane (20) and the via signal barrel (10), such that the first anti-pad (400, 500, 600) has a first orientation and a first void (210). The method further includes forming a second anti-pad (400', 500', 600') positioned between the second conductive plane (20') and the via signal barrel (10), such that the second anti-pad (400', 500', 600') has a second orientation and a second void (210'). The first orientation is offset from the second orientation and the first void (210) does not completely overlap the second void (210'). See *Specification*, at page 8, line 5 through page 11, line 2; and Figures 6-10.

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

- I. Whether claims 1-31 are patentable under 35 U.S.C. § 103(a) over the Oggioni et al., U.S. Patent No. 6,710,258.

ARGUMENT**I. The Applicable Law**

With regard to a 35 U.S.C. § 103 obviousness rejection: "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." M.P.E.P. 2141 (emphasis in the original). The Examiner bears the burden under 35 U.S.C. § 103 in establishing a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *In re Fine* at 1074. Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375, 379 (Fed. Cir. 1986). Third, the reference or combined references must teach or suggest all of the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A. 1974).

The court in *Fine* stated:

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Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."

In re Fine, 5 USPQ2d at 1599 (citations omitted).

There must be some teaching somewhere that provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem that it addresses. *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988); *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (C.C.P.A. 1979). In particular, "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based upon applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142 (emphasis added).

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). Furthermore, claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), *cert. denied*, 481 U.S. 1052 (1987). At the same time, a prior patent cited as a § 103 reference must be considered in its entirety, "*i.e.* as a *whole*, including portions that lead away from the invention." *Id.* That is, the Examiner must recognize and consider not only the similarities, but also the critical differences between the claimed invention and the prior art as one of the factual inquiries pertinent to any obviousness inquiry under 35 U.S.C. § 103. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990) (emphasis added). Finally, the Examiner must avoid hindsight. *Id.*

With regard for the test for obviousness under § 103, a statement that modifications of the prior art to meet the claimed invention would have been "'well within the ordinary skill of the art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to

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combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993); M.P.E.P. § 2143.01 (emphasis in the original).

In conclusion, an applicant is entitled to a patent grant if any one of the elements of a *prima facie* case of obviousness is not established. The Federal Circuit has endorsed this view in stating: "If examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1448 (Fed. Cir. 1992).

II. Rejection of claims 1-31 under 35 U.S.C. § 103(a) as being unpatentable over the Oggioni et al., US. Patent No. 6,710,258.

The Oggioni et al. patent fails to render claims 1-31 *prima facie* obvious.

Appellant submits that the Oggioni et al. patent fails to teach or suggest the invention of independent claim 1. Independent claim 1 includes the limitation "wherein the first voided area does not completely overlap the second voided area." The Examiner admits that the Oggioni et al. patent does not specifically state that the first voided area does not completely overlap the second voided area. The Examiner submits, however, that the Oggioni et al. patent:

teaches that when the dielectric layers of the PCB are different thicknesses, each of the "anti-pad" can be individually crafted to achieve the desired impedance matching (see col. 4, lines 50 – col. 5, line 20). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the anti-pads in the invention of Oggioni et al. such that the voids do not completely overlap. The motivation for doing so would have been to provide equivalent shielding in layers having different dielectric thicknesses. (Final Office Action mailed December 12, 2005, page 3).

In addition, in the Response to Arguments section, the Examiner states:

However, in this individual crafting it is entirely reasonable that the ordinarily skilled artisan, motivated to satisfy specific requirements (col. 8, lines 35-45) would construct the first and second voided areas to not overlap completely. Moreover, such a modification would also be considered a change of form of the device, and it has been held that more than a mere change of form is necessary for patentability. *Span-Deck, Inc. v. Fab-con, Inc.* (CA 8, 1982) 215 USPQ 835. (Final Office Action mailed December 12, 2005, page 8).

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Individually crafting the anti-pads to achieve the desired impedance matching does not teach or suggest that the first voided area does not completely overlap the second voided area as recited in independent claim 1. Impedance matching is not affected by the overlapping of voided areas. The Oggioni et al. patent figures and text do not provide any indication that the first voided area does not completely overlap the second voided area. Instead, the Oggioni et al. patent figures illustrate that the voided areas are aligned.

In addition, the limitation of independent claim 1 of wherein the first voided area does not completely overlap the second voided area is not merely a change in form, but provides advantages and new and unexpected results not suggested by the Oggioni et al. patent. The invention as recited by independent claim 1 addresses planarity issues associated with anti-pads. For example, with reference to Figure 6:

Partially voided anti-pads 400 and 400' maintain the planarity of the PCB by preventing dielectric material from settling into voids 210 and 210' left when anti-pads 400 and 400' are formed. This is accomplished by leaving some conductive material 200 and 200' behind to support the dielectric material. Modifying the orientation of patterned partially voided anti-pads 400 and 400' from conductive plane 20 to conductive plane 20' provides additional support to maintain board planarity. Anti-pads 400 and 400' are oriented so that void 210 on conductive plane 20 is at least partially supported by conducting material 200' on conductive plane 20'. Stated another way, voided areas 210 and 210' do not completely overlap each other. The surface area of anti-pads 400 and 400' can therefore be increased in size by increasing the amount of conductive material removed. The increased support of the layered structure and the increased voided surface area of anti-pads 400 and 400' reduce the stray capacitance while maintaining board planarity." (Specification, page 8, lines 14-28).

The Oggioni et al. patent does not teach or suggest fabricating the rings to prevent non-planarity of a PCB. Rather, the Oggioni et al. patent is directed to reducing stray capacitance associated with a via-hole without losing the shielding effect provided by the rings. (Abstract). In the Oggioni et al. patent, planarity of the PCB is not listed as a requirement that must be considered when fabricating the rings. Therefore, one skilled in the art would not look to the Oggioni et al. patent for fabricating anti-pads for preventing non-planarity of a PCB. Preventing non-planarity of a PCB is not an expected or inherent result of practicing the Oggioni et al. patent. Accordingly, independent claim 1 is believed to be allowable over the Oggioni et al. patent.

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Independent claims 8, 15, and 24 all include the limitation "wherein the first orientation is offset from the second orientation." The Examiner admits that the Oggioni et al. patent does not specifically state that the first orientation is offset from the second orientation. The Examiner provides similar reasons as to the rejection to independent claim 1 based on the Oggioni et al. patent teaching that when the dielectric layers of the PCB are different thicknesses, each of the anti-pads can be individually crafted to achieve the desired impedance matching.

Similar to reasons discussed above with reference to independent claim 1, individually crafting the anti-pads to achieve the desired impedance matching does not teach or suggest that the first orientation is offset from the second orientation. Impedance matching is not affected by the first orientation being offset from the second orientation as recited in independent claims 8, 15, and 24. The Oggioni et al. patent figures and text do not provide any indication that the first orientation is offset from the second orientation. Instead, the Oggioni et al. patent figures illustrate that the first orientation of the first partially voided anti-pad is aligned with the second orientation of the second partially voided anti-pad, such that the voided areas are aligned.

In addition, as previously discussed above with reference to independent claim 1, the limitations of independent claims 8, 15, and 24 of wherein the first orientation is offset from the second orientation is not merely a change in form, but provides advantages and new and unexpected results not suggested by the Oggioni et al. patent. The invention as recited by independent claims 8, 15, and 24 addresses planarity issues associated with anti-pads. One skilled in the art would not look to the Oggioni et al. patent for fabricating anti-pads for preventing non-planarity of a PCB. Preventing non-planarity of a PCB is not an expected or inherent result of practicing the Oggioni et al. patent. Therefore, independent claims 8, 15, and 24 are believed to be allowable over the Oggioni et al. patent.

Dependent claims 2-7 further define patentably distinct independent claim 1. Dependent claims 9-14 further define patentably distinct independent claim 8. Dependent claims 16-23 further define patentably distinct independent claim 15. Dependent claims 25-31 further define patentably distinct independent claim 24. Accordingly, these dependent claims are also believed to be allowable over the Oggioni et al. patent.

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In addition, the Oggioni et al. patent fails to teach or suggest the first and second anti-pads are longer in a first direction than in a second direction (claim 4); wherein the first pattern comprises a screen pattern (claims 14 and 30); wherein the first length and the first width are not equal (claim 16); wherein the second length and the second width are not equal (claim 17); wherein the first length substantially equals the second length and the first width equals the second width (claim 20); wherein the first and second anti-pads are substantially oval shaped (claims 21 and 26); and wherein the first orientation is substantially perpendicular to the second orientation (claim 22).

The Oggioni et al. patent states that the arrangement of the via-hole at the center of the rings ensures that no asymmetry is introduced. (Col. 5, lines 49-51). By contrast, the shapes defined in dependent claims 4, (14 and 30), 16, 17, 20, (21 and 26), and 22 introduce asymmetry. In addition, while the Oggioni et al. patent states that the rings may be comprised of square or other polygonal shape frames (col. 6, lines 7-8), the Oggioni et al. patent fails to teach or suggest the defined shapes and/or patterns of dependent claims 4, (14-30), 16, 17, 20, (21 and 26), and 22 that provide new and unexpected results in preventing non-planarity of a PCB.

Further, the Oggioni et al. patent fails to teach or suggest "wherein the first and third orientations are substantially identical and adapted to allow a signal trace between the first and third anti-pads on an adjacent signal plane" as recited by dependent claim 23.

The Oggioni et al. patent does not disclose anti-pads having different orientations or adjacent anti-pads having substantially identical orientations adapted to allow a signal trace between the anti-pads on an adjacent signal plane as recited by dependent claim 23. The orientation of the anti-pads, as defined by dependent claim 23, provides new and unexpected results. For example, with reference to figure 9:

To maintain signal integrity through signal trace 710 on a PCB, signal trace 710 can be placed on a signal layer immediately above or below a non-voided area of conductive plane 20. If signal trace 710 is routed above or below a voided area of conductive plane 20, such as above or below the voided area of anti-pad 600, noise can be introduced into signal trace 710 during circuit operation. If several anti-pads 600 situated close together are formed too large, conductive plane 20 between anti-pads 600 can be choked off which prevents the routing of signal traces 710 between anti-pads 600 on adjacent signal layers. Elongated anti-pads 600 allow signal traces 710 to be routed in

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at least one direction between anti-pads 600 while still increasing the size of anti-pads 600. (Specification, page 10, lines 11-20).

One skilled in the art would not look to the Oggioni et al. patent for fabricating anti-pads in a manner defined by dependent claim 23 to allow signal traces between the anti-pads on an adjacent signal plane. The fabrication of anti-pads to fulfill this purpose is not an expected or inherent result of practicing the Oggioni et al. patent.

In view of the above, Appellant respectfully requests reversal of the rejection of claims 1-31 under 35 U.S.C. §103(a).

CONCLUSION

For the above reasons, Appellant respectfully submits that the cited references neither anticipate nor render obvious claims of the pending Application. The pending claims distinguish over the cited references, and therefore, Appellant respectfully submits that the rejection must be withdrawn, and respectfully requests the Examiner be reversed and claims 1-31 be allowed.

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Any inquiry regarding this Appeal Brief should be directed to either Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005 or David Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854 or. In addition, all correspondence should continue to be directed to the following address:

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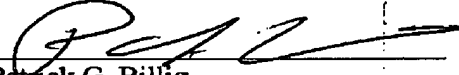
Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously Presented) A printed circuit board comprising:
 - a first conductive plane;
 - a second conductive plane substantially parallel to the first conductive plane;
 - a via signal barrel transecting the first and second conductive planes;
 - a first anti-pad positioned between the first conductive plane and the via signal barrel, the first anti-pad having a first voided area and a first non-voided area; and
 - a second anti-pad positioned between the second conductive plane and the via signal barrel, the second anti-pad having a second voided area and a second non-voided area;wherein the first voided area does not completely overlap the second voided area.
2. (Original) The printed circuit board of claim 1, wherein the first conductive plane comprises one of a power plane and a ground plane.
3. (Original) The printed circuit board of claim 1, wherein the second conductive plane comprises one of a power plane and a ground plane.
4. (Original) The printed circuit board of claim 1, wherein the first and second anti-pads are longer in a first direction than in a second direction.
5. (Original) The printed circuit board of claim 1, wherein the first and second anti-pads are partially voided anti-pads.
6. (Original) The printed circuit board of claim 1, wherein the first and second anti-pads are configured to maintain board planarity.
7. (Original) The printed circuit board of claim 1, wherein the first and second anti-pads are configured for signals through the via signal barrel greater than approximately 2 GHz.
8. (Original) A printed circuit board comprising:

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Title: ALTERNATING VOIDED AREAS OF ANTI-PADS

a first conductive plane;
a second conductive plane substantially parallel to the first conductive plane;
a via signal barrel transecting the first and second conductive planes;
a first partially voided anti-pad positioned between the first conductive plane and the via signal barrel, the first partially voided anti-pad having a first pattern and a first orientation; and
a second partially voided anti-pad positioned between the second conductive plane and the via signal barrel, the second partially voided anti-pad having a second pattern and a second orientation;
wherein the first orientation is offset from the second orientation.

9. (Original) The printed circuit board of claim 8, wherein the first and second partially voided anti-pads are configured to maintain planarity of the printed circuit board.

10. (Original) The printed circuit board of claim 8, wherein the first and second patterns are substantially identical.

11. (Original) The printed circuit board of claim 8, wherein the first and second partially voided anti-pads are configured for signals through the via signal barrel greater than approximately 2 GHz.

12. (Original) The printed circuit board of claim 8, wherein the first pattern comprises one of a symmetric pattern and an asymmetric pattern.

13. (Original) The printed circuit board of claim 8, wherein the first pattern comprises one of a concentric circles pattern, a radial spokes pattern, and an arbitrary pattern.

14. (Original) The printed circuit board of claim 8, wherein the first pattern comprises a screen pattern.

15. (Original) A printed circuit board comprising:

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a first conductive plane;
a second conductive plane substantially parallel to the first conductive plane;
a first via signal barrel transecting the first and second conductive planes;
a first anti-pad positioned between the first conductive plane and the first via signal barrel, the first anti-pad having a first length and a first width and a first orientation; and
a second anti-pad positioned between the second conductive plane and the first via signal barrel, the second anti-pad having a second length and a second width and a second orientation;
wherein the first orientation is offset from the second orientation.

16. (Original) The printed circuit board of claim 15, wherein the first length and the first width are not equal.

17. (Original) The printed circuit board of claim 15, wherein the second length and the second width are not equal.

18. (Original) The printed circuit board of claim 15, wherein the first and second anti-pads are configured to maintain planarity of the printed circuit board.

19. (Original) The printed circuit board of claim 15, wherein the first and second anti-pads are configured for signals through the first via signal barrel greater than approximately 2 GHz.

20. (Original) The printed circuit board of claim 15, wherein the first length substantially equals the second length and the first width equals the second width.

21. (Original) The printed circuit board of claim 15, wherein the first and second anti-pads are substantially oval shaped.

22. (Original) The printed circuit board of claim 15, wherein the first orientation is substantially perpendicular to the second orientation.

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23. (Original) The printed circuit board of claim 15, further comprising:

a second via signal barrel parallel to the first via signal barrel and transecting the first and second conductive planes;

a third anti-pad positioned between the second via signal barrel and the first conductive plane, the third anti-pad having a third orientation; and

a fourth anti-pad positioned between the second via signal barrel and the second conductive plane, the fourth anti-pad having a fourth orientation;

wherein the first and third orientations are substantially identical and adapted to allow a signal trace between the first and third anti-pads on an adjacent signal plane.

24. (Original) A method for forming a printed circuit board, comprising:

providing a first conductive plane;

providing a second conductive plane substantially parallel to the first conductive plane;

forming a via signal barrel transecting the first and second conductive planes;

forming a first anti-pad positioned between the first conductive plane and the via signal barrel, such that the first anti-pad has a first orientation and a first void; and

forming a second anti-pad positioned between the second conductive plane and the via signal barrel, such that the second anti-pad has a second orientation and a second void;

wherein the first orientation is offset from the second orientation; and

wherein the first void does not completely overlap the second void.

25. (Original) The method of claim 24, wherein the first and second anti-pads are configured to maintain planarity of the printed circuit board.

26. (Original) The method of claim 24, wherein the first and second anti-pads are substantially oval shaped.

27. (Original) The method of claim 24, wherein the first and second anti-pads are partially voided in a pattern.

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28. (Original) The method of claim 27, wherein the pattern comprises one of a symmetric pattern and an asymmetric pattern.

29. (Original) The method of claim 27, wherein the pattern comprises one of a concentric circles pattern, a radial spokes pattern, and an arbitrary pattern.

30. (Original) The method of claim 27, wherein the pattern comprises a screen pattern.

31. (Original) The method of claim 24, wherein the first and second anti-pads are configured for signals through the via signal barrel greater than approximately 2 GHz.

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EVIDENCE APPENDIX

None.

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RELATED PROCEEDINGS APPENDIX

None.

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